REMARKS

Claims 1-13, 18-26, 57-62 are pending in the present application. Claims 1-13, 18-26 and 57-61 stand rejected under 35 U.S.C. §112, first paragraph. Claims 1-13 and 57-58 stand rejected under 35 U.S.C. §112, second paragraph. Claims 57-58 stand rejected under 35 U.S.C. §102(b) for anticipation by U.S. Patent No. 5,475,317 to Smith. Claims 1 and 18 stand rejected under 35 U.S.C. §102(b) for anticipation by U.S. Patent No. 5,378,311 to Nagayama et al.

Applicant respectfully traverses the rejections and urges allowance of the present application.

Turning to independent claim 1, a wafer processing apparatus comprises, in part, a wafer holder adapted to receive a wafer having an electrical coupling and the wafer holder including an electrical coupling configured to electrically couple with the electrical coupling of the wafer and communicate signals between the wafer and the wafer holder. Claim 1 recites patentable subject matter over the prior art of record.

Paragraph 5 on page 4 of the Office Action identifies teachings which allegedly correspond to limitations of independent claim 1. It is stated that the wafer holder 51 includes electrical couplings 57-63 for coupling to the wafer. Thereafter, it is stated that it appears that the wafer *inherently* has electrical coupling in which the electrical couplings of the holder connected thereto. Applicant asserts the teachings of the Nagayama reference fail to anticipate or render obvious positively recited limitations of claim 1.

Referring to the teachings in column 2, line 57 to column 3, line 50, exemplary

operations of components 57-63 of Nagayama are described. Voltage sources 59 and 60 are operable to apply respective positive and negative DC voltage to an internal electrode 53. It is stated that negative charges are induced to the surface of wafer 54 upon connection of DC power source 60. An RF power source 63 is connected to the wafer stage 55 to apply an RF bias producing ion energy. DC power source 59 is connected to electrode 53 to apply a positive DC voltage shown in Fig. 1B.

Such teachings illustrate inducement of an electric charge upon a surface of wafer 54 and application of RF bias during etching. It is clearly stated that electrode 53 is buried within insulation member 52. Such construction fails to teach or suggest an electrical coupling of the wafer holder configured to electrically couple with the electrical coupling of the wafer. Mere inducement of surface charge upon a surface of a wafer fails to teach or suggest an electrical coupling of a wafer holder being configured to electrically couple with an electrical coupling of the wafer.

Further, such teachings fail to disclose or suggest *communication of signals between the wafer and the wafer holder* as specifically defined in claim 1. Inducement of negative charge upon the surface of the wafer 54 holds the wafer upon chuck 51 by a coulomb force. The RF source provides RF bias producing predetermined incident ion energy. Such teachings in no fair interpretation disclose or suggest communication of signals between the wafer and the wafer holder as recited in claim 1. Claim 1 recites limitations not shown or suggested in the prior art of record and is in condition for allowance for at least this reason.

In addition, Applicant objects to the statement that the wafer inherently has

electrical coupling. In relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics *necessarily* flows from the teachings of the applied prior art. *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). No structure corresponding to an electrical coupling of the wafer is disclosed, suggested, or necessarily flows from the teachings of the prior art. The Nagayama reference merely discloses a wafer with no structure corresponding to the positively claimed electrical coupling of the wafer. Claim 1 is patentable over the prior art for at least this additional reason.

The claims which depend from independent claim 1 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

Claim 18 recites a wafer processing apparatus comprising, in part, a wafer holder having circuitry configured to communicate a process signal received from a wafer and the process signal containing information regarding processing of the wafer. Claim 18 recites patentable subject matter over the prior art of record.

Mere inducement of a surface charge upon a wafer or application of an RF bias for etching fails to disclose or suggest the claimed wafer holder having *circuitry configured to communicate a process signal received from a wafer and the process signal containing information regarding processing of the wafer* as defined in claim 18. Electrical signals of Nagayama provide an attractive force of the wafer as well as RF bias energy for etching and fail to include any information regarding processing of a wafer. Claim 18 recites limitations not shown or suggested in the prior art of record and is in condition for

allowance for at least this reason.

Referring to claim 57, an electronic device workpiece processing apparatus comprises, in part, a workpiece holder including a vacuum chamber adapted to receive a vacuum to couple a received electronic device workpiece with the workpiece holder. Claim 57 recites patentable subject matter over the prior art of record.

Referring to page 4 of the Office Action, teachings of the Smith reference are identified which allegedly correspond to limitations of Applicant's claims. Applicant notes that the Office Action is entirely devoid of identifying any reference teachings which allegedly correspond to the claimed vacuum chamber of claim 57. Applicant has electronically searched the Smith reference and has failed to uncover any vacuum chamber teachings. Positively recited limitations of claim 57 are not shown or suggested in the prior art of record and claim 57 is allowable for at least this reason.

Independent claim 58 defines an electronic device workpiece processing apparatus comprising, in part, a workpiece holder including an electrical coupling configured to extend outward from plural surfaces of the workpiece holder, and a contact plate. Claim 58 recites patentable subject matter over the prior art of record.

The Office Action fails to identify any teachings of the Smith patent which allegedly correspond to the electrical coupling of the workpiece holder configured to extend outward from plural surfaces of the workpiece holder as specifically defined. The Smith reference fails to teach or suggest positively recited limitations of claim 58 and claim 58 is allowable for at least this reason.

Referring to the 35 U.S.C. §112, first paragraph rejections, Applicant has deleted

the language identified by the Examiner pursuant to the telephonic interview between the undersigned and the Examiner. Such claims comply with the first paragraph of section 112.

Referring to the 35 U.S.C. §112, second paragraph rejections, Figs. 2 and 3 disclosing different wafer holder configurations. The claimed wafer holder is understood by one of skill in the art. Applicant has amended claims 8 and 9 as indicated. An exemplary vacuum chamber is depicted as reference 49 in Fig. 2 of the originally filed application. Claims 53 and 54 have been canceled. Claim 58 has been amended to delete the conductive column language. Applicant submits all pending claims are definite and in compliance with 35 U.S.C. §112, second paragraph.

Applicant submits herewith a copy of a form PTO-1449 having references thereon which have not been initialed by the Examiner. Applicant respectfully requests initialization of all references upon such form and return of the initialed form to Applicant.

Applicant respectfully requests allowance of all pending claims.

The Examiner is requested to phone the undersigned if the Examiner believes such would facilitate prosecution of the present application. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: 9/26/01

By: _____

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Group Art Unit 2832
Examiner . . . . . V. Nguyen
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Title: "Wafer Processing Apparatuses and Electronic Device Workpiece Processing Apparatuses (As Amended)"

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO JUNE 26, 2001 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

1. (Twice Amended) A wafer processing apparatus comprising:

a wafer holder adapted to receive a wafer having an electrical coupling ~~and to expose the wafer to a chemical processing environment to chemically process the wafer~~, the wafer holder including an electrical coupling configured to electrically couple with the electrical coupling of the wafer and communicate signals between the wafer and the wafer holder.

8. (Twice Amended) The wafer processing apparatus according to claim 1 wherein the wafer holder comprises a chuck configured to receive one of a calibration wafer and a production wafer.

9. (Twice Amended) The wafer processing apparatus according to claim 8 wherein the wafer holder ~~and the calibration wafer include~~ includes vacuum chambers adapted to receive a vacuum to couple one of the calibration wafer and the production wafer with the chuck.

18. (Twice Amended) A wafer processing apparatus comprising:

a wafer holder ~~adapted to receive a wafer and to expose the wafer to a chemical processing environment to chemically process the wafer, the wafer holder~~ having circuitry configured to communicate a process signal received from a ~~received~~ wafer and the process signal containing information regarding processing of the ~~received~~ wafer.

19. (Twice Amended) A wafer processing apparatus comprising:

a chuck including a surface, an electrical coupling adjacent the surface, and electrical interconnect configured to connect with the electrical coupling of the chuck and conduct a signal within the chuck;

an intermediate member adapted to receive a wafer and ~~to expose the wafer to a chemical processing environment to chemically process the wafer,~~ the intermediate member having a first surface and a second surface and the intermediate member including:

an electrical coupling adjacent the first surface and configured to couple with the electrical coupling of the chuck;

an electrical coupling adjacent the second surface; and

an electrical interconnect configured to connect the electrical coupling adjacent the first surface and the electrical coupling adjacent the second surface; and

a wafer configured to couple with the second surface of the intermediate member, the wafer including a sensor and an electrical coupling configured to provide electrical connection of the sensor with the electrical coupling of the second surface of the intermediate member.

26. (Twice Amended) A wafer processing apparatus comprising:

a chuck including a surface, a plurality of electrical couplings adjacent the surface, and a plurality of electrical interconnects configured to connect with respective electrical couplings of the chuck and conduct signals within the chuck;

an intermediate member adapted to receive a wafer and ~~to expose the wafer to a chemical processing environment to chemically process the wafer,~~ the intermediate member having a first surface and a second surface and the intermediate member including:

a plurality of electrical couplings adjacent the first surface and configured to couple with respective electrical couplings of the chuck;

a plurality of electrical couplings adjacent the second surface; and

a plurality of electrical interconnects configured to electrically connect the electrical couplings of the first surface with respective electrical couplings of the second surface;

a calibration wafer configured to couple with the second surface of the intermediate member, the calibration wafer including a plurality of resistance temperature devices configured to generate process signals, and a plurality of electrical connections configured to electrically connect the resistance temperature devices with respective electrical couplings of the second surface of the intermediate member; and

a data gathering device coupled with the electrical interconnects of the chuck and configured to receive the process signals from the resistance temperature devices through the intermediate member and the chuck.

58. (Amended) An electronic device workpiece processing apparatus comprising:

a workpiece holder adapted to receive an electronic device workpiece having an electrical coupling, the workpiece holder including an electrical coupling configured to electrically couple with the electrical coupling of the electronic device workpiece and communicate signals between the electronic device workpiece and the workpiece holder, wherein the electrical coupling of the workpiece holder ~~comprises a conductive column~~ is configured to extend outward from plural surfaces of the workpiece holder; and

a contact plate including circuitry configured to provide electrical connection with the conductive column.